



A62S8308 Series

Preliminary

256K X 8 BIT LOW VOLTAGE CMOS SRAM

Document Title

256K X 8 BIT LOW VOLTAGE CMOS SRAM

Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Issue Date</u>	<u>Remark</u>
0.0	Initial issue	December 6, 1999	Preliminary
0.1	Modify Vccmax from 3.3V to 3.6V	December 20, 2000	
0.2	Add 55ns grade spec. for VCC = 3.0V to 3.6V	March 23, 2001	



A62S8308 Series

Preliminary

256K X 8 BIT LOW VOLTAGE CMOS SRAM

Features

- Power supply range: 2.7V to 3.6V
- Access times: 55ns (max.): for VCC = 3.0V to 3.6V
70ns (max.): for VCC = 2.7V to 3.6V
- Current:
 - A62S8308-S series: Operating: 40mA (max.)
Standby: 10μA (max.)
 - A62S8308-SI series: Operating: 40mA (max.)
Standby: 15μA (max.)
- Extended operating temperature range:-25°C to 85°C for -SI series

- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL compatible
- Common I/O using three-state output
- Output enable and two chip enable inputs for easy application
- Data retention voltage: 2V (min.)
- Available in 32-pin SOP, TSOP, sTSOP (8X 13.4mm) forward type and 36-ball Mini BGA (6X8) packages

General Description

The A62S8308 is a low operating current 2,097,152-bit static random access memory organized as 262,144 words by 8 bits and operates on a low power supply voltage from 2.7V to 3.6V.

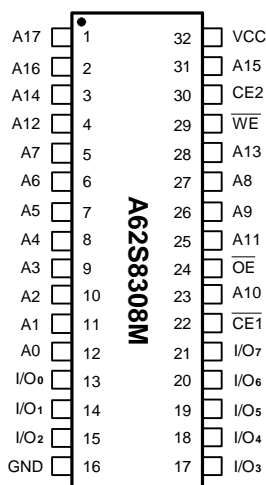
Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

Two chip enable inputs are provided for power down and a device enable and an output enable input are included for easy interfacing.

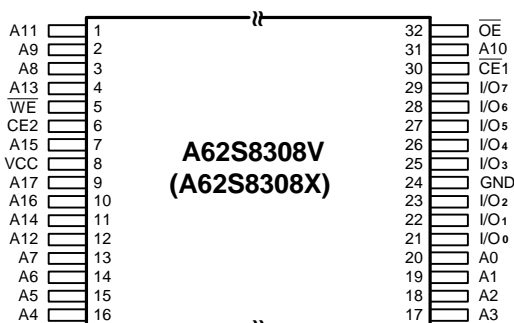
Data retention is guaranteed at a power supply voltage as low as 2V.

Pin Configurations

■ SOP

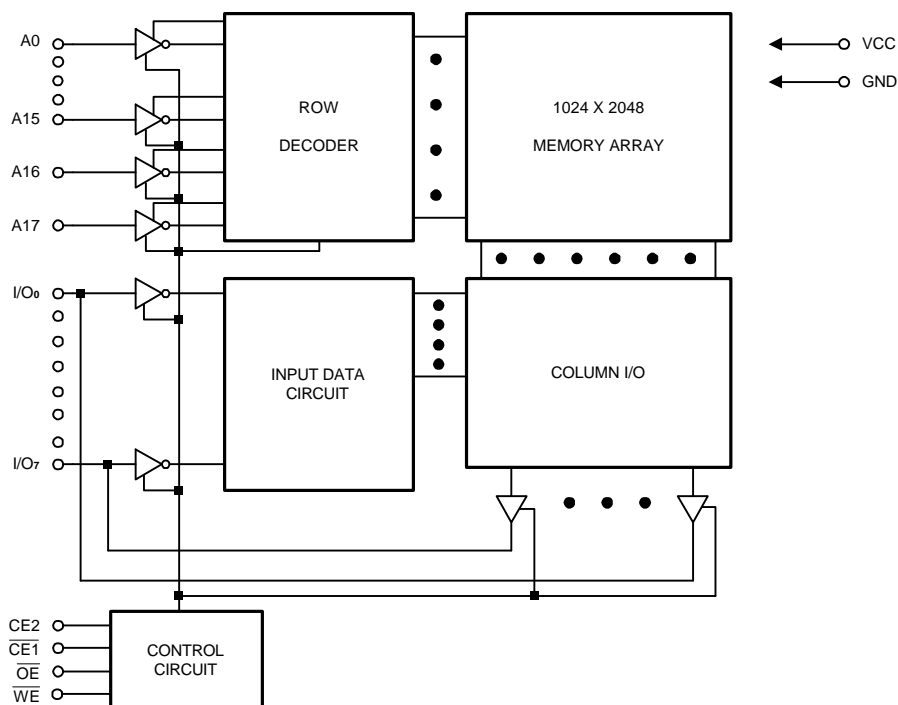


■ TSOP/(sTSOP) (forward type)



■ Mini BGA (6X8) Top View

	1	2	3	4	5	6
A	A0	A1	CE2	A3	A6	A8
B	I/O4	A2	WE	A4	A7	I/O0
C	I/O5		NC	A5		I/O1
D	VSS					VCC
E	VCC					VSS
F	I/O6		NC	A17		I/O2
G	I/O7	OE	CE1	A16	A15	I/O3
H	A9	A10	A11	A12	A13	A14

Block Diagram

Pin Descriptions - SOP

Pin No.	Symbol	Description
1 - 12, 23, 25 - 28, 31	A0 - A17	Address Inputs
13 - 15, 17 - 21	I/O ₀ - I/O ₇	Data Inputs/Outputs
16	GND	Ground
22	$\overline{\text{CE1}}$	Chip Enable 1
24	$\overline{\text{OE}}$	Output Enable
29	$\overline{\text{WE}}$	Write Enable
30	CE2	Chip Enable 2
32	VCC	Power Supply

Pin Description - TSOP/sTSOP

Pin No.	Symbol	Description
1 - 4, 7, 9 - 20, 31	A0 - A17	Address Inputs
5	$\overline{\text{WE}}$	Write Enable
6	CE2	Chip Enable 2
8	VCC	Power Supply
21 - 23, 25 - 29	I/O ₀ - I/O ₇	Data Inputs/Outputs
24	GND	Ground
30	$\overline{\text{CE1}}$	Chip Enable 1
32	$\overline{\text{OE}}$	Output Enable

Recommended DC Operating Conditions
 $(T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C or } -25^{\circ}\text{C to } 85^{\circ}\text{C})$

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	2.7	3.0	3.6	V
GND	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.4	-	VCC + 0.3	V
V _{IL}	Input Low Voltage	-0.3	-	+0.6	V
C _L	Output Load	-	-	30	pF
TTL	Output Load	-	-	1	-

Absolute Maximum Ratings*

VCC to GND -0.5V to + 4.6V
 IN, IN/OUT Volt to GND -0.5V to VCC + 0.5V
 Operating Temperature, Topr -25°C to + 85°C
 Storage Temperature, Tstg -55°C to + 125°C
 Power Dissipation, Pr 0.7W
 Soldering Temp. & Time 260°C, 10 sec

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics $(T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C or } -25^{\circ}\text{C to } 85^{\circ}\text{C, VCC} = 2.7\text{V to } 3.6\text{V, GND} = 0\text{V})$

Symbol	Parameter	A62S8308-55S/70S		A62S8308-55SI/70SI		Unit	Conditions
		Min.	Max.	Min.	Max.		
I _{LI}	Input Leakage Current	-	1	-	1	μA	V _{IN} = GND to VCC
I _{LO}	Output Leakage Current	-	1	-	1	μA	$\overline{\text{CE1}} = V_{IH}$ or $\text{CE2} = V_{IL}$ or $\overline{\text{OE}} = V_{IH}$ or $\text{WE} = V_{IL}$ V _{IO} = GND to VCC
I _{CC}	Active Power Supply Current	-	3	-	3	mA	$\overline{\text{CE1}} = V_{IL}$, CE2 = V _{IH} I _{VO} = 0mA
I _{CC1}	Dynamic Operating Current	-	40	-	40	mA	Min. Cycle, Duty = 100% $\overline{\text{CE1}} = V_{IL}$, CE2 = V _{IH} I _{VO} = 0mA
I _{CC2}		-	10	-	10	mA	$\overline{\text{CE1}} = V_{IL}$, CE2 = V _{IH} V _{IH} = VCC, V _{IL} = 0V, f = 1MHz, I _{VO} = 0mA

DC Electrical Characteristics (continued)

Symbol	Parameter	A62S8308-55S/70S		A62S8308-55SI/70SI		Unit	Conditions
		Min.	Max.	Min.	Max.		
I_{SB}	Standby Power Supply Current	-	0.5	-	0.5	mA	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$
I_{SB1}		-	10	-	15	μA	$\overline{CE1} \geq V_{CC} - 0.2V$ $CE2 \geq V_{CC} - 0.2V$ $V_{IN} \geq 0V$
I_{SB2}		-	10	-	15	μA	$CE2 \leq 0.2V$ $V_{IN} \geq 0V$
V_{OL}	Output Low Voltage	-	0.4	-	0.4	V	$I_{OL} = 2.1mA$
V_{OH}	Output High Voltage	2.4	-	2.4	-	V	$I_{OH} = -1.0mA$

Truth Table

Mode	$\overline{CE1}$	CE2	\overline{OE}	\overline{WE}	I/O Operation	Supply Current
Standby	H	X	X	X	High Z	I_{SB}, I_{SB1}
	X	L	X	X	High Z	I_{SB}, I_{SB2}
Output Disable	L	H	H	H	High Z	I_{CC}, I_{CC1}, I_{CC2}
Read	L	H	L	H	D _{OUT}	I_{CC}, I_{CC1}, I_{CC2}
Write	L	H	X	L	D _{IN}	I_{CC}, I_{CC1}, I_{CC2}

Note: X = H or L

Capacitance ($T_A = 25^\circ C$, $f = 1.0MHz$)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}^*	Input Capacitance		6	pF	$V_{IN} = 0V$
C_{IO}^*	Input/Output Capacitance		8	pF	$V_{IO} = 0V$

* These parameters are sampled and not 100% tested.

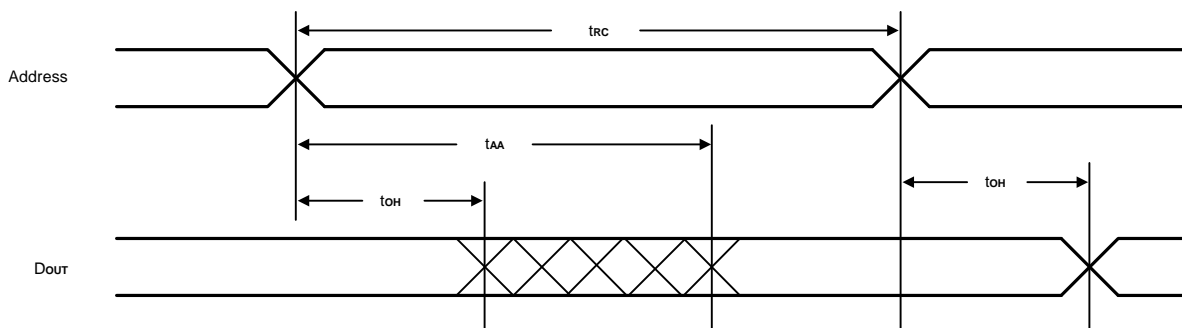
AC Characteristics ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ or -25°C to 85°C , $V_{CC} = 2.7\text{V}$ to 3.6V)

Symbol	Parameter		A62S8308-55S/SI (VCC = 3.0V to 3.6V)		A62S8308-70S/SI (VCC = 2.7V to 3.6V)		Unit
			Min.	Max.	Min.	Max.	
Read Cycle							
t _{RC}	Read Cycle Time		55	-	70	-	ns
t _{AA}	Address Access Time		-	55	-	70	ns
t _{ACE1}	Chip Enable Access Time	$\overline{\text{CE1}}$	-	55	-	70	ns
t _{ACE2}		CE2	-	55	-	70	ns
t _{OE}	Output Enable to Output Valid		-	30	-	35	ns
t _{CLZ1}	Chip Enable to Output in Low Z	$\overline{\text{CE1}}$	10	-	10	-	ns
t _{CLZ2}		CE2	10	-	10	-	ns
t _{OLZ}	Output Enable to Output in Low Z		5	-	5	-	ns
t _{CHZ1}	Chip Disable to Output in High Z	$\overline{\text{CE1}}$	0	20	0	25	ns
t _{CHZ2}		CE2	0	20	0	25	ns
t _{OHZ}	Output Disable to Output in High Z		0	20	0	25	ns
t _{OH}	Output Hold from Address Change		5	-	10	-	ns
Read Cycle							
t _{WC}	Write Cycle Time		55	-	70	-	ns
t _{CW}	Chip Enable to End of Write		50	-	60	-	ns
t _{AS}	Address Setup Time		0	-	0	-	ns
t _{AW}	Address Valid to End of Write		50	-	60	-	ns
t _{WP}	Write Pulse Width		40	-	50	-	ns
t _{WR}	Write Recovery Time		0	-	0	-	ns
t _{WHZ}	Write to Output in High Z		0	25	0	25	ns
t _{DW}	Data to Write Time Overlap		25	-	30	-	ns
t _{DH}	Data Hold from Write Time		0	-	0	-	ns
t _{OW}	Output Active from End of Write		5	-	5	-	ns

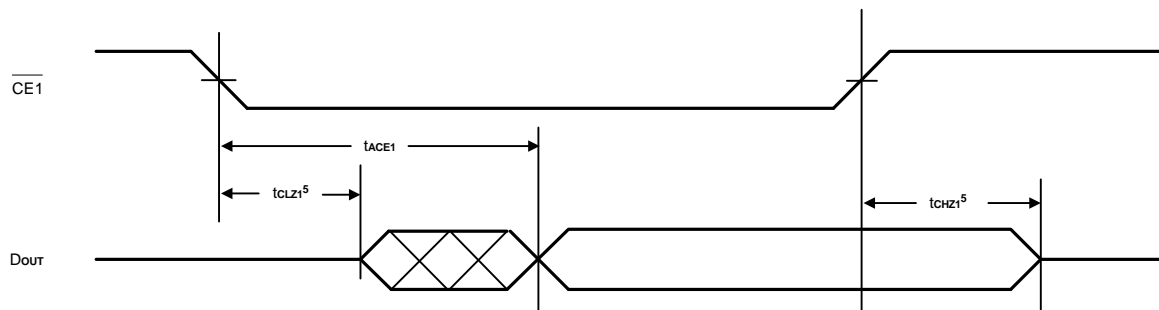
Notes: t_{CHZ1}, t_{CHZ2}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

Timing Waveforms

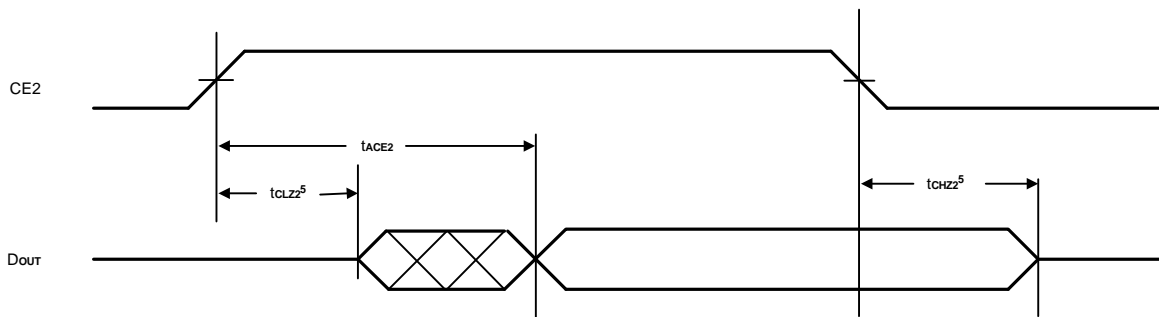
Read Cycle 1^(1, 2, 4)

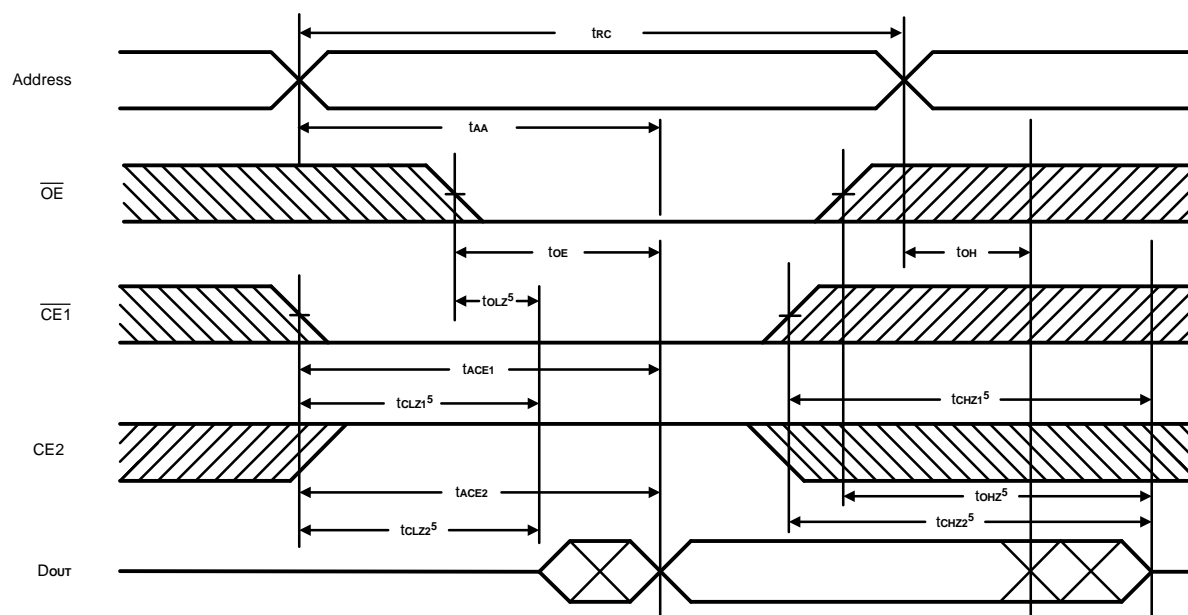


Read Cycle 2^(1, 3, 4, 6)

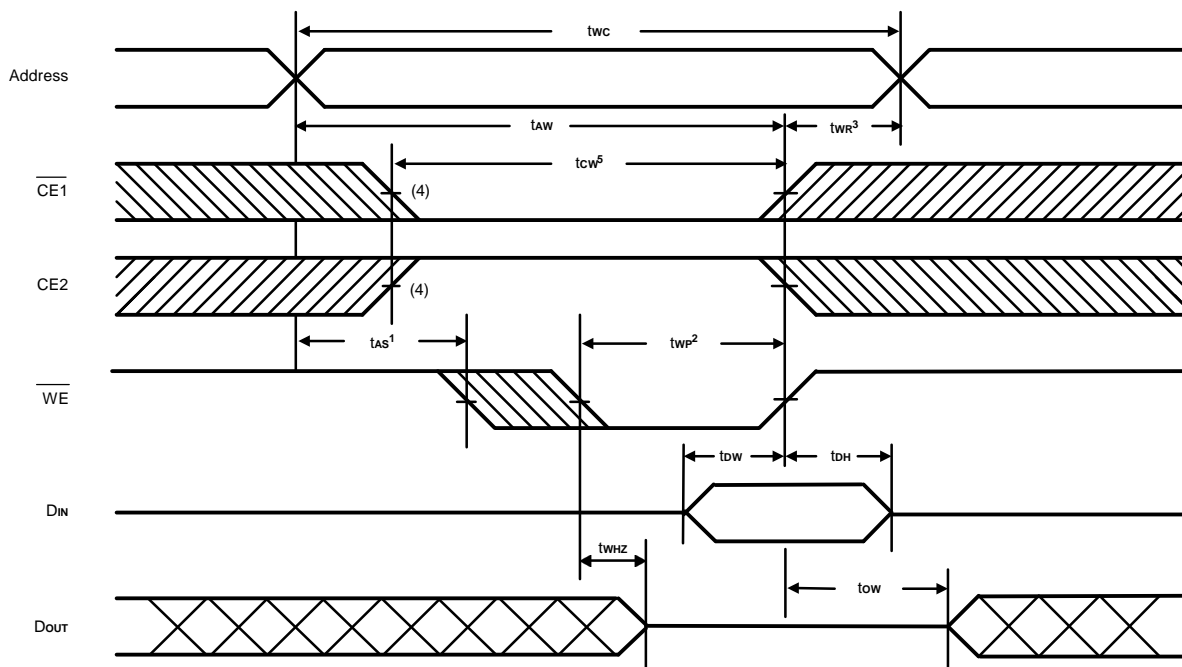


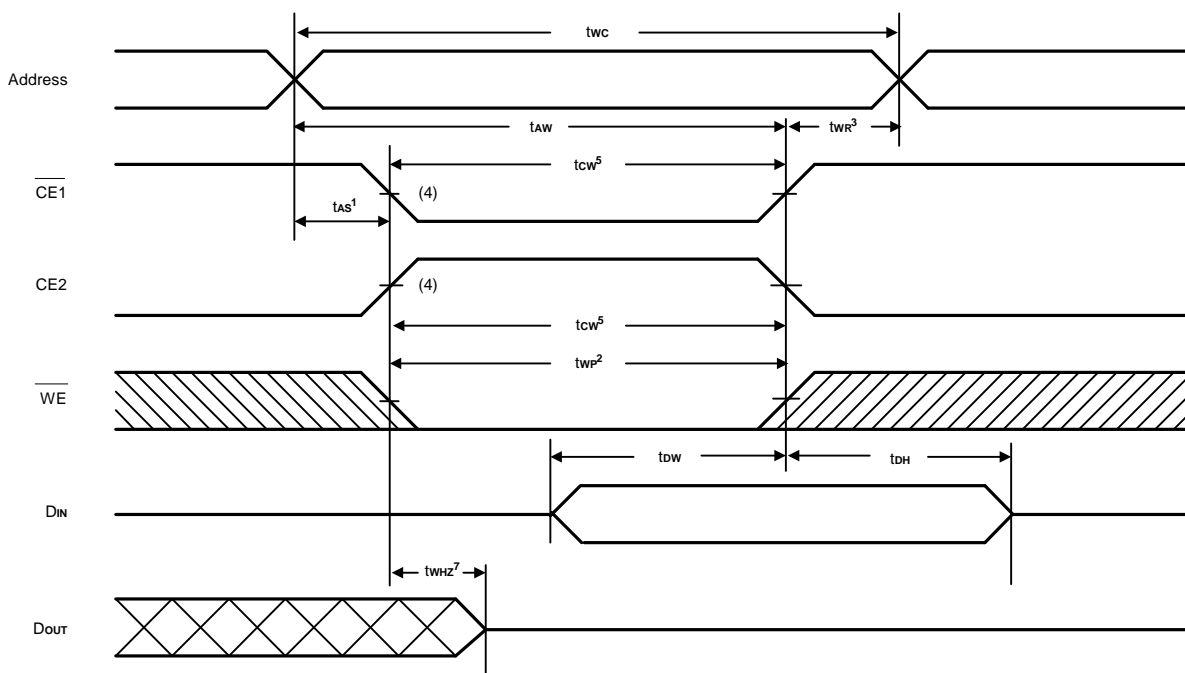
Read Cycle 3^(1, 4, 7, 8)



Timing Waveforms (continued)
Read Cycle 4 ⁽¹⁾


- Notes:
1. \overline{WE} is high for Read Cycle.
 2. Device is continuously enabled $\overline{CE1} = V_{IL}$ and $\overline{CE2} = V_{IH}$.
 3. Address valid prior to or coincident with $\overline{CE1}$ transition low.
 4. $\overline{OE} = V_{IL}$.
 5. Transition is measured $\pm 500\text{mV}$ from steady state. This parameter is sampled and not 100% tested.
 6. $\overline{CE2}$ is high.
 7. $\overline{CE1}$ is low.
 8. Address valid prior to or coincident with $\overline{CE2}$ transition high.

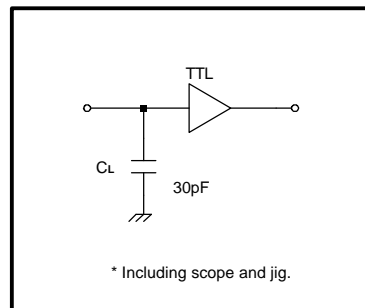
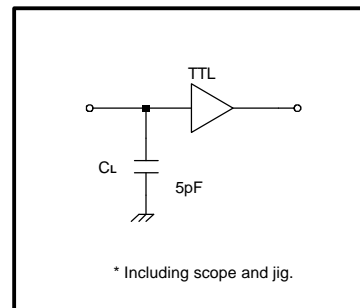
Timing Waveforms (continued)
Write Cycle 1⁽⁶⁾
(Write Enable Controlled)


Timing Waveforms (continued)
Write Cycle 2
(Chip Enable Controlled)


- Notes:
1. t_{as} is measured from the address valid to the beginning of Write.
 2. A Write occurs during the overlap (t_{wp}) of a low $\overline{CE1}$, a high CE2 and a low \overline{WE} .
 3. t_{wr} is measured from the earliest of $\overline{CE1}$ or \overline{WE} going high or CE2 going low to the end of the Write cycle.
 4. If the $\overline{CE1}$ low transition or the CE2 high transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} transition, outputs remain in a high impedance state.
 5. t_{cw} is measured from the later of $\overline{CE1}$ going low or CE2 going high to the end of Write.
 6. \overline{OE} is continuously low. ($\overline{OE} = V_{IL}$)
 7. Transition is measured $\pm 500\text{mV}$ from steady state. This parameter is sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figures 1 and 2


Figure 1. Output Load

Figure 2. Output Load for t_{CLZ1} , t_{CLZ2} , t_{OHZ} , t_{OLZ} , t_{CHZ1} , t_{CHZ2} , t_{WHZ} , and t_{OW}
Data Retention Characteristics ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ or -25°C to 85°C)

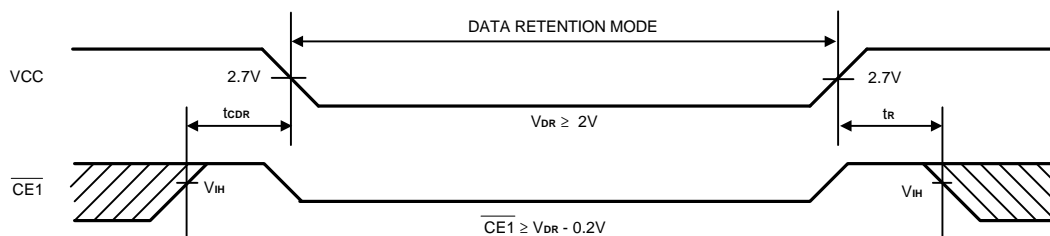
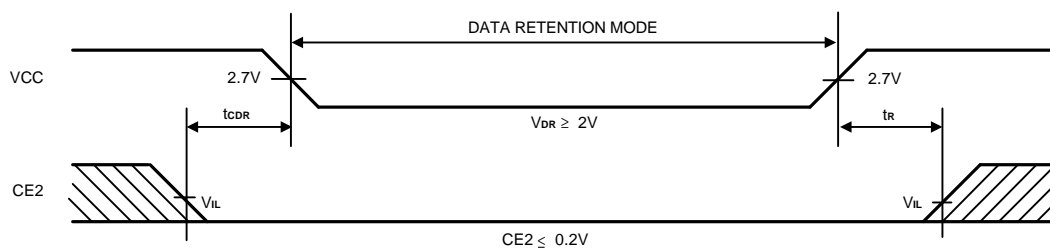
Symbol	Parameter		Min.	Max.	Unit	Conditions
V_{DR1}	VCC for Data Retention		2.0	3.6	V	$\overline{CE1} \geq V_{CC} - 0.2V$
V_{DR2}			2.0	3.6	V	$\overline{CE2} \leq 0.2V$ $\overline{CE1} \geq V_{CC} - 0.2V$ or $\overline{CE1} \leq 0.2V$
I_{CCDR1}	Data Retention Current	S-Version	-	5*	μA	$V_{CC} = 2.0V$ $\overline{CE1} \geq V_{CC} - 0.2V$ $\overline{CE2} \geq V_{CC} - 0.2V$ $V_{IN} \geq 0V$
		SI-Version	-	10**		
I_{CCDR2}		S-Version	-	5*	μA	$V_{CC} = 2.0V$ $\overline{CE2} \leq 0.2V$ $V_{IN} \geq 0V$
		SI-Version	-	10**		
t_{CDR}	Chip Disable to Data Retention Time		0	-	ns	See Retention Waveform
t_R	Operation Recovery Time		t_{RC}	-	ns	

* A62S8308-55S/70S

I_{CCDR} : Max. $1\mu A$ at $T_A = 0^\circ\text{C} + 40^\circ\text{C}$

** A62S8308-55SI/70SI

I_{CCDR} : Max. $1\mu A$ at $T_A = 0^\circ\text{C} + 40^\circ\text{C}$

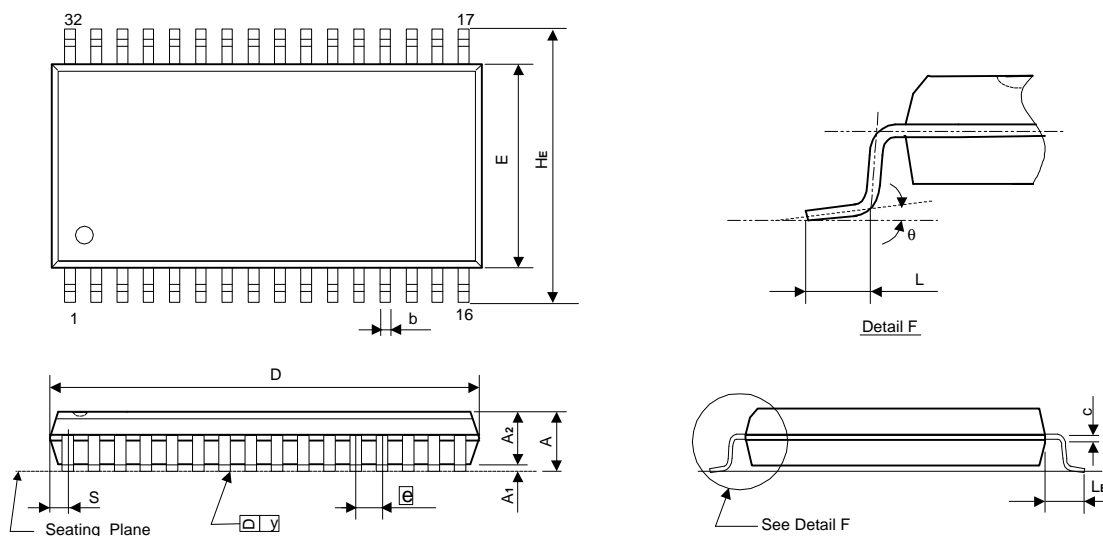
Low VCC Data Retention Waveform (1) ($\overline{\text{CE1}}$ Controlled)

Low VCC Data Retention Waveform (2) (CE2 Controlled)


Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (μA)	Package
A62S8308M-55S	55	40	10	32L SOP
A62S8308M-55SI		40	15	32L SOP
A62S8308V-55S		40	10	32L TSOP
A62S8308V-55SI		40	15	32L TSOP
A62S8308X-55S		40	10	32L sTSOP
A62S8308X-55SI		40	15	32L sTSOP
A62S8308G-55S		40	10	36B Mini BGA
A62S8308G-55SI		40	15	36B Mini BGA
A62S8308M-70S	70	40	10	32L SOP
A62S8308M-70SI		40	15	32L SOP
A62S8308V-70S		40	10	32L TSOP
A62S8308V-70SI		40	15	32L TSOP
A62S8308X-70S		40	10	32L sTSOP
A62S8308X-70SI		40	15	32L sTSOP
A62S8308G-70S		40	10	36B Mini BGA
A62S8308G-70SI		40	15	36B Mini BGA

Package Information
SOP (W.B.) 32L Outline Dimensions

unit: inches/mm



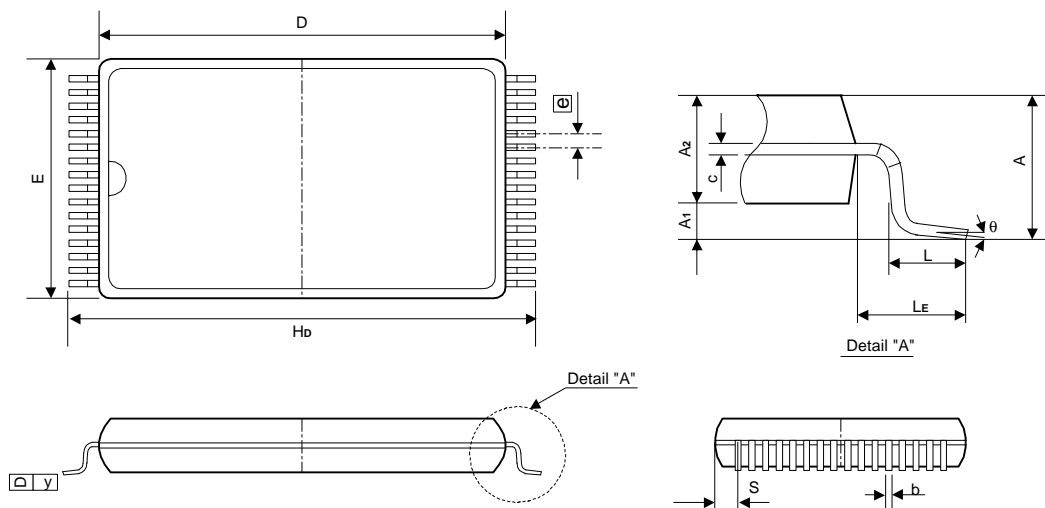
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.118	-	-	3.00
A1	0.004	-	-	0.10	-	-
A2	0.101	0.106	0.111	2.57	2.69	2.82
b	0.014	0.016	0.020	0.36	0.41	0.51
c	0.006	0.008	0.012	0.15	0.20	0.31
D	-	0.805	0.817	-	20.45	20.75
E	0.440	0.445	0.450	11.18	11.30	11.43
e	0.044	0.050	0.056	1.12	1.27	1.42
HE	0.546	0.556	0.566	13.87	14.12	14.38
L	0.023	0.031	0.039	0.58	0.79	0.99
LE	0.047	0.055	0.063	1.19	1.40	1.60
S	-	-	0.036	-	-	0.91
y	-	-	0.004	-	-	0.10
θ	0°	-	10°	0°	-	10°

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.

Package Information
TSOP 32L TYPE I (8 X 20mm) Outline Dimensions

unit: inches/mm



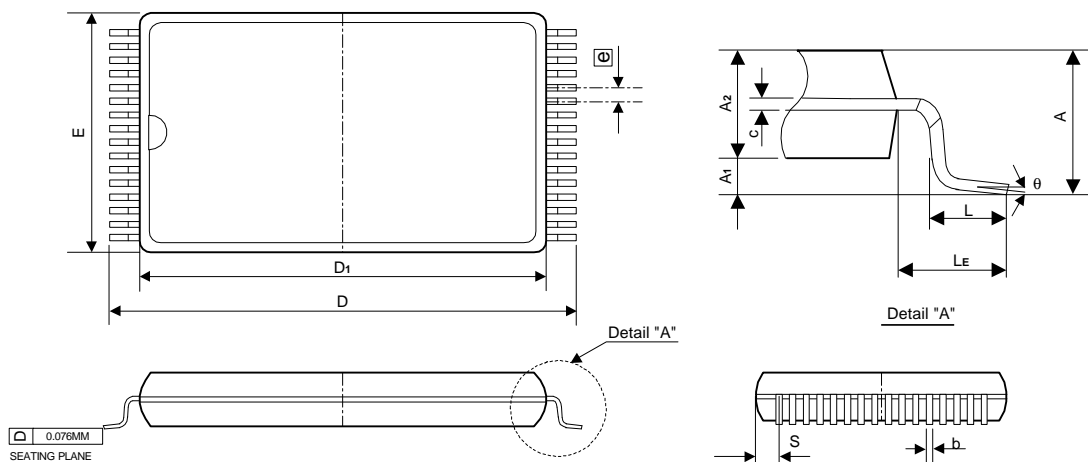
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.047	-	-	1.20
A ₁	0.002	-	0.006	0.05	-	0.15
A ₂	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.009	0.011	0.18	0.22	0.27
c	0.004	-	0.008	0.11	-	0.20
D	0.720	0.724	0.728	18.30	18.40	18.50
E	-	0.315	0.319	-	8.00	8.10
e	0.020 BSC			0.50 BSC		
Hb	0.779	0.787	0.795	19.80	20.00	20.20
L	0.016	0.020	0.024	0.40	0.50	0.60
LE	-	0.032	-	-	0.80	-
S	-	-	0.020	-	-	0.50
y	-	-	0.003	-	-	0.08
θ	0°	-	5°	0°	-	5°

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.

Package Information
sTSOP 32L TYPE I (8 X 13.4mm) Outline Dimensions

unit: inches/mm



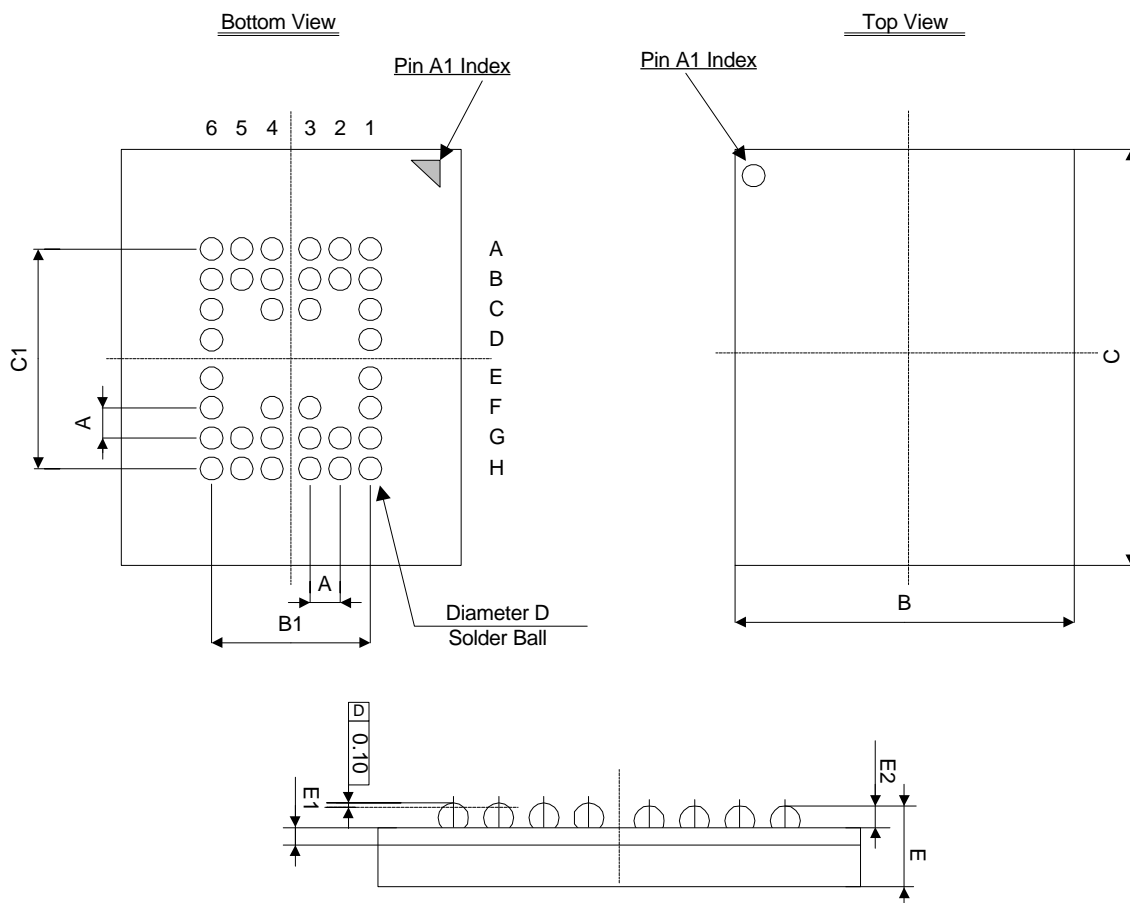
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.049	-	-	1.25
A1	0.002	-	-	0.05	-	-
A2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.008	0.009	0.17	0.20	0.23
c	0.0056	0.0059	0.0062	0.142	0.150	0.158
E	0.311	0.315	0.319	7.90	8.00	8.10
e	0.020 TYP			0.50 TYP		
D	0.520	0.528	0.535	13.20	13.40	13.60
D1	0.461	0.465	0.469	11.70	11.80	11.90
L	0.012	0.020	0.028	0.30	0.50	0.70
LE	0.0275	0.0315	0.0355	0.700	0.800	0.900
S	0.0109 TYP			0.278 TYP		
theta	0°	3°	5°	0°	3°	5°

Notes:

1. The maximum value of dimension D1 includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.

Package Information
Mini BGA 6X8 (36 BALLS) Outline Dimensions

unit : millimeter(mm)



Symbol	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	1.00	1.10	1.20
E1	-	0.36	-
E2	-	0.22	-